

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT125**

**Quad buffer/line driver; 3-state**

Product specification  
File under Integrated Circuits, IC06

December 1990

## Quad buffer/line driver; 3-state

## 74HC/HCT125

### FEATURES

- Output capability: bus driver
- $I_{CC}$  category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT125 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT125 are four non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs (nY) are controlled by the output enable input (nOE). A HIGH at nOE causes the outputs to assume a HIGH impedance OFF-state.

The "125" is identical to the "126" but has active LOW enable inputs.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

| SYMBOL            | PARAMETER                                | CONDITIONS                                   | TYPICAL |     | UNIT |
|-------------------|--|--|---------|-----|------|
|                   |  |  | HC      | HCT |      |
| $t_{PHL}/t_{PLH}$ | propagation delay nA to nY               | $C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$ | 9       | 12  | ns   |
| $C_I$             | input capacitance                        |  | 3.5     | 3.5 | pF   |
| $C_{PD}$          | power dissipation capacitance per buffer | notes 1 and 2                                | 22      | 24  | pF   |

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

### ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

| PIN NO.      | SYMBOL                               | NAME AND FUNCTION                  |
|--------------|--------------------------------------|------------------------------------|
| 1, 4, 10, 13 | $\overline{1OE}$ to $\overline{4OE}$ | outputs enable inputs (active LOW) |
| 2, 5, 9, 12  | 1A to 4A                             | data inputs                        |
| 3, 6, 8, 11  | 1Y to 4Y                             | data outputs                       |
| 7            | GND                                  | ground (0 V)                       |
| 14           | $V_{CC}$                             | positive supply voltage            |

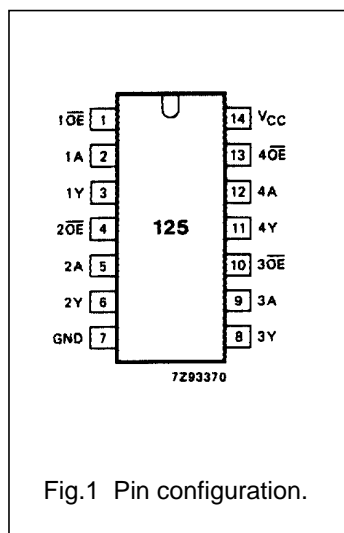


Fig.1 Pin configuration.

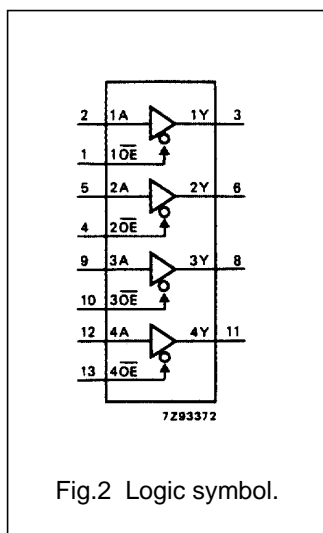


Fig.2 Logic symbol.

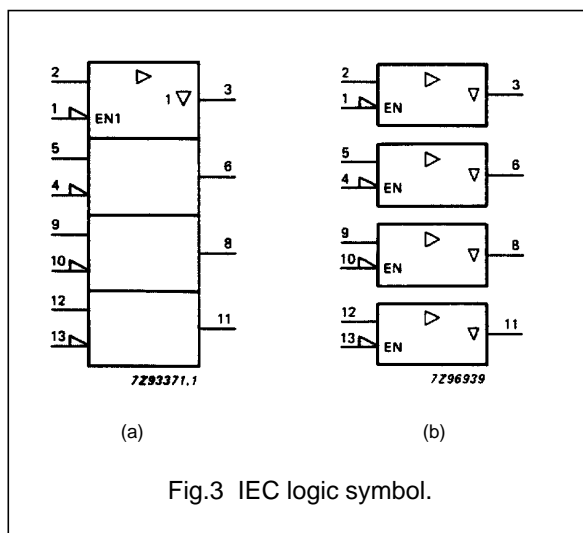


Fig.3 IEC logic symbol.

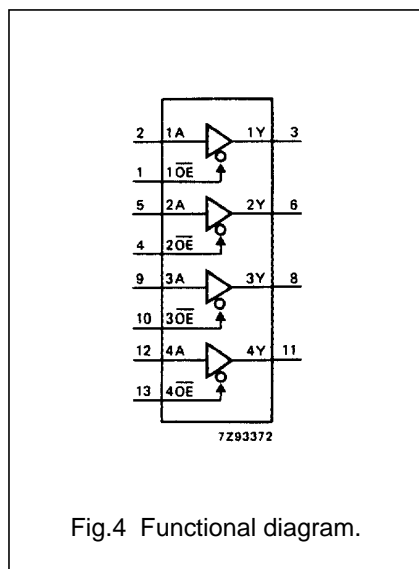


Fig.4 Functional diagram.

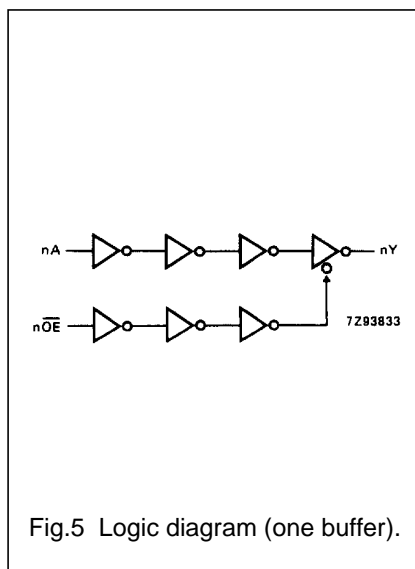


Fig.5 Logic diagram (one buffer).

FUNCTION TABLE

| INPUTS           |    | OUTPUT |
|------------------|----|--------|
| $n\overline{OE}$ | nA | nY     |
| L                | L  | L      |
| L                | H  | H      |
| H                | X  | Z      |

Note

1. H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state

## Quad buffer/line driver; 3-state

## 74HC/HCT125

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER                                | T <sub>amb</sub> (°C) |                |                 |            |                 |             | UNIT            | TEST CONDITIONS        |                   |       |
|-------------------------------------|--|-----------------------|----------------|-----------------|------------|-----------------|-------------|-----------------|------------------------|-------------------|-------|
|                                     |  | 74HC                  |                |                 |            |                 |             |                 | V <sub>CC</sub><br>(V) | WAVEFORMS         |       |
|                                     |  | +25                   |                |                 | -40 to +85 |                 | -40 to +125 |                 |                        |                   |       |
|                                     |  | min.                  | typ.           | max.            | min.       | max.            | min.        |                 |                        |                   | max.  |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nA to nY            |                       | 30<br>11<br>9  | 100<br>20<br>17 |            | 125<br>25<br>21 |             | 150<br>30<br>26 | ns                     | 2.0<br>4.5<br>6.0 | Fig.6 |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable time<br>nOE to nY  |                       | 41<br>15<br>12 | 125<br>25<br>21 |            | 155<br>31<br>26 |             | 190<br>38<br>32 | ns                     | 2.0<br>4.5<br>6.0 | Fig.7 |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable time<br>nOE to nY |                       | 41<br>15<br>12 | 125<br>25<br>21 |            | 155<br>31<br>26 |             | 190<br>38<br>32 | ns                     | 2.0<br>4.5<br>6.0 | Fig.7 |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                   |                       | 14<br>5<br>4   | 60<br>12<br>10  |            | 75<br>15<br>13  |             | 90<br>18<br>15  | ns                     | 2.0<br>4.5<br>6.0 | Fig.6 |

## Quad buffer/line driver; 3-state

## 74HC/HCT125

**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT                 | UNIT LOAD COEFFICIENT |
|-----------------------|-----------------------|
| nA, n $\overline{OE}$ | 1.00                  |

**AC CHARACTERISTICS FOR 74HCT**

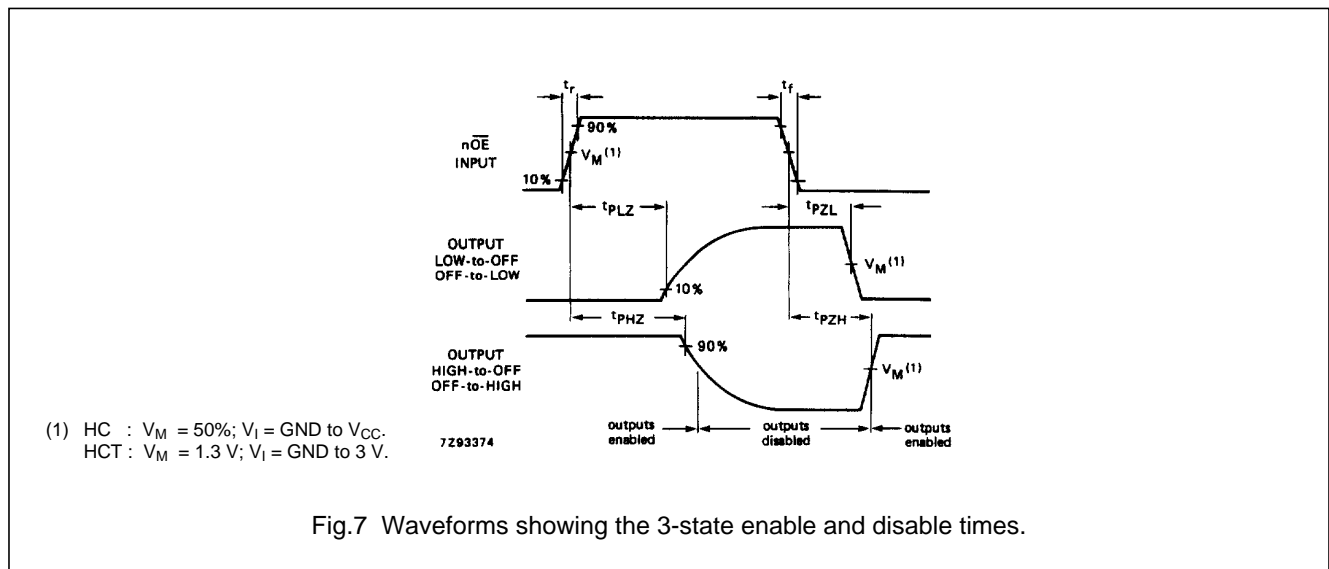
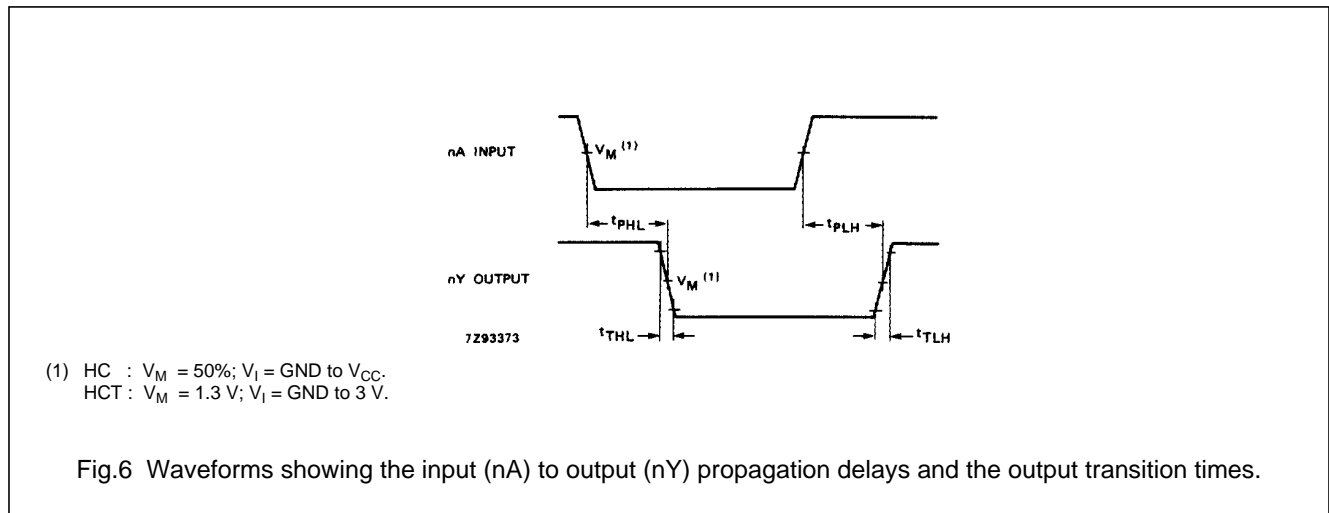
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER  | T <sub>amb</sub> (°C) |      |      |            |      |             | UNIT | TEST CONDITIONS        |           |       |
|-------------------------------------|--|-----------------------|------|------|------------|------|-------------|------|------------------------|-----------|-------|
|                                     |  | 74HCT                 |      |      |            |      |             |      | V <sub>CC</sub><br>(V) | WAVEFORMS |       |
|                                     |  | +25                   |      |      | -40 to +85 |      | -40 to +125 |      |                        |           |       |
|                                     |  | min.                  | typ. | max. | min.       | max. | min.        |      |                        |           | max.  |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nA to nY                          |                       | 15   | 25   |            | 31   |             | 38   | ns                     | 4.5       | Fig.6 |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable time<br>n $\overline{OE}$ to nY  |                       | 15   | 28   |            | 35   |             | 42   | ns                     | 4.5       | Fig.7 |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable time<br>n $\overline{OE}$ to nY |                       | 15   | 25   |            | 31   |             | 38   | ns                     | 4.5       | Fig.7 |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time                                 |                       | 5    | 12   |            | 15   |             | 18   | ns                     | 4.5       | Fig.6 |

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".